Shri Phanishwar Nath Renu Engineering College, Araria

(Under Department of Science & Technology Patna, Govt. of Bihar)

Ref. No: SPNREC/900
Room No: 01

Date: 13/12/2023
W.E. F: 18.12.2023

Time Table, SPNREC ARARIA
5thSEM, Electronics & Communication ENGINEERING

	Period 1	Period 2	Period 3		Period 4	Period 5	Period 6
Day	**10:00–11:00**	**11.00–12.00**	**12:00–1:00**	**1:00-2:00**	**2:00-3:00**	**3:00-4:00**	**4.00-5:00**
Mon	Linear Integrated Circuit	Digital Signal Processing	Microprocessor & Microcontroller	LUNCH BREAK	Linear Control System	Microprocessor & Microcontroller Lab	
Tue	Probability & Stochastic Processes	Linear Control System	Digital Signal Processing		Linear Integrated Circuit Lab		COI
Wed	Linear Integrated Circuit	Digital Signal Processing	GATE		Linear Control System -	Computer Network & Security	EVS
Thu	Linear Integrated Circuit	Linear Control System	Probability & Stochastic Processes		Microprocessor & Microcontroller	EVS	Computer Network & Security
Fri	Computer Network & Security	GATE	Microprocessor & Microcontroller		Digital Signal Processing Lab		EVS
Sat	COI	Probability & Stochastic Processes	**GATE**		Internship& Software Skills		Library

Course Title	Faculty Name
Digital Signal Processing (T+P)	Prof. Priyatam Kumar, Asst Prof. ECE
Linear Integrated Circuit (T+P)	Prof. Amit Ranjan Asst Prof. ECE, Prof. Kumar Vimal Asst Prof. ECE
Microprocessor & Microcontroller(T+P)	Prof. Shahin, Asst Prof. ECE
Constitution of India (COI)	Prof. Kumar Vimal Asst Prof. ECE, Prof. Raj Kumar Sharma Asst Prof. ECE
Environmental Science	Prof. Sriram Yadav, GAP
Linear Control System	Prof. Dharmendra Kumar, Asst. Prof. ECE
Probability & Stochastic Processes	Prof. Bikky Kumar, Asst. Prof. Math, Dr Ritesh Kumar Asst. Prof. ECE
Computer Network & Security	Prof.. SriramYadav, GAP
Internship & Software Skills	Prof. Kumar Vimal, Asst. Prof. ECE

KV 13/12/2023
Professor I/C
Time Table

13.12.2023
Principal
SPNREC ARARIA